



Phase Control Thyristor

DS5933-4 April 2013 (LN30253)

FEATURES

- Double Side Cooling
- High Surge Capability

KEY PARAMETERS

V _{DRM}	6500V
I _{T(AV)}	3310A
I _{TSM}	44200A
dV/dt*	2000V/µs
dl/dt	200A/µs

* Higher dV/dt selections available

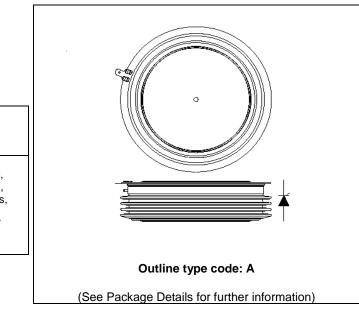


Fig. 1 Package outline

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V _{DRM} and V _{RRM} V	Conditions
DCR3220A65* DCR3220A60 DCR3220A55	6500 6000 5500	$\begin{array}{l} T_{vj} = -40^{\circ}C \ to \ 125^{\circ}C, \\ I_{DRM} = I_{RRM} = 300mA, \\ V_{DRM}, \ V_{RRM} \ t_p = 10ms, \\ V_{DSM} \ \& \ V_{RSM} = \\ V_{DRM} \ \& \ V_{RRM} \ + \ 100V \\ respectively \end{array}$

Lower voltage grades available. *6200V @ -40° C, 6500V @ 0° C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR3220A65

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.



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CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions		Units
Double Sid	de Cooled			
I _{T(AV)}	Mean on-state current	Half wave resistive load	3220	А
I _{T(RMS)}	RMS value	-	5058	А
Ι _Τ	Continuous (direct) on-state current	-	4655	А

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}C$	43.0	kA
l ² t	I ² t for fusing	V _R = 0	9.25	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R _{th(j-c)}	Thermal resistance – junction to case	Double side cooled	DC	-	0.00603	°C/W
		Single side cooled	Anode DC	-	0.01024	°C/W
			Cathode DC	-	0.01467	°C/W
R _{th(c-h)}	Thermal resistance – case to heatsink	Clamping force 83.0kN	Double side	-	0.001	°C/W
		(with mounting compound)	Single side	-	0.002	°C/W
T_{vj}	Virtual junction temperature	Blocking V _{DRM} / V _{RRM}		-	125	°C
T _{stg}	Storage temperature range			-55	125	°C
F _m	Clamping force			74.0	91.0	kN

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DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I _{RRM} /I _{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125°C	At V _{RRM} /V _{DRM} , T _{case} = 125°C		300	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V _{DRM} , T _j = 125°C, ga	ate open	-	2000	V/µs
dl/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω ,	Non-repetitive	-	500	A/µs
		t _r < 0.5µs, T _j = 125°C				
V _{T(TO)}	Threshold voltage – Low level	500 to 1900A at T _{case} = 125°	С	-	1.01	V
	Threshold voltage – High level	1900 to 6000A at T _{case} = 125	°C	-	1.08	V
r⊤	On-state slope resistance – Low level	500A to 1900A at $T_{case} = 125$	5°C	-	0.3	mΩ
	On-state slope resistance – High level	1600A to 6000A at T _{case} = 125°C		-	0.2643	mΩ
t _{gd}	Delay time	V _D = 67% V _{DRM} , gate source	30V, 10Ω	-	3	μs
		$t_r = 0.5 \mu s, T_j = 25^{\circ}C$				
tq	Turn-off time	$I_T = 3000A, T_j = 125^{\circ}C,$ $V_R = 200V, dI/dt = 1A/\mu s,$			500	μs
		$dV_{DR}/dt = 20V/\mu s$ linear				
Qs	Stored charge	I⊤ = 3000A, T _i = 125°C, dl/dt – 1A/μs,		3830	6430	μC
I _{RR}	Reverse recovery current	$V_{\text{Rpeak}} \sim 3900\text{V}, V_{\text{R}} \sim 2600\text{V}$		45	60	A
ΙL	Latching current	$T_j = 25^{\circ}C, V_D = 5V$		-	3	A
I _H	Holding current	$T_j = 25^{\circ}C, R_{G-K} = \infty, I_{TM} = 500$	0A, I _T = 5A	-	300	mA

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GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V _{DRM} , T _{case} = 125°C	0.4	V
I _{GT}	Gate trigger current	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	400	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM} , T _{case} = 125°C	10	mA

CURVES

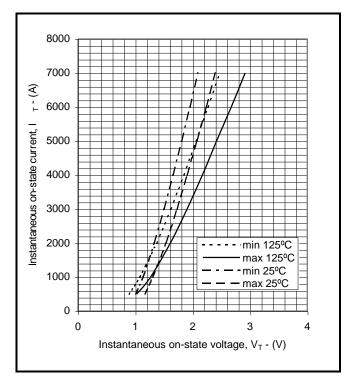


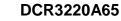
Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

 $V_{TM} = A + BIn (I_T) + C.I_T + D.\sqrt{I_T}$

Where A = -0.645429 B = 0.3001939 C = 0.000276 D = - 0.01259 these values are valid for T_j = 125°C for I_T 500A to 6000A





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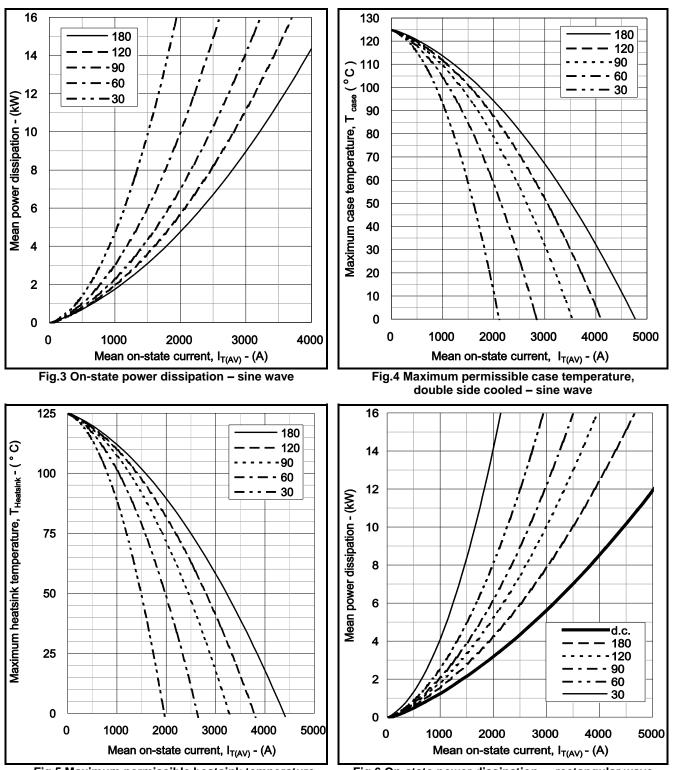


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave



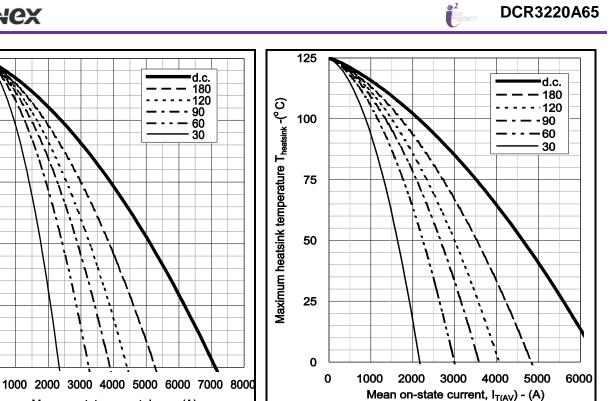


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Maximum permissible case temperature , T_{case} -(° C) 57 00 00

0

0



Mean on-state current. IT(A) - (A) Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

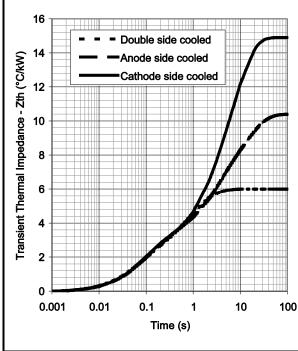


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

		1	2	3	4
Double side cooled	R _i (°C/kW)	3.01541	1.048955	0.983519	0.983519
Double side cooled	T _i (s)	0.703874	1.904794	0.059	0.059
Anode side cooled	R _i (°C/kW)	3.156003	4.092806	1.556555	1.623962
Anode side cooled	T _i (s)	2.69023	13.79162	0.059	0.205916
Cathode side cooled	R _i (°C/kW)	7.077369	3.483481	1.745839	2.634274
Cambue side cooled	T _i (s)	6.648601	8.436484	1.762119	0.08069

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T/T_i))]$$

 $\Delta R_{th(j-c)}$ Conduction

The show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Do	Double side cooling		Ar	Anode Side Cooling			Cathode Sided Cooling		
	ΔZ_{th}	(z)		ΔZ	_h (z)			ΔZ	_{th} (z)
θ°	sine.	rect.	θ°	sine.	rect.	θ	•	sine.	rect.
180	0.44	0.31	180	0.42	0.30	18	30	0.42	0.30
120	0.49	0.43	120	0.47	0.41	12	20	0.47	0.41
90	0.55	0.49	90	0.52	0.46	9	0	0.52	0.46
60	0.60	0.55	60	0.57	0.52	6	0	0.57	0.52
30	0.64	0.61	30	0.61	0.58	3	0	0.60	0.58
15	0.66	0.64	15	0.62	0.61	1	5	0.62	0.60

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)



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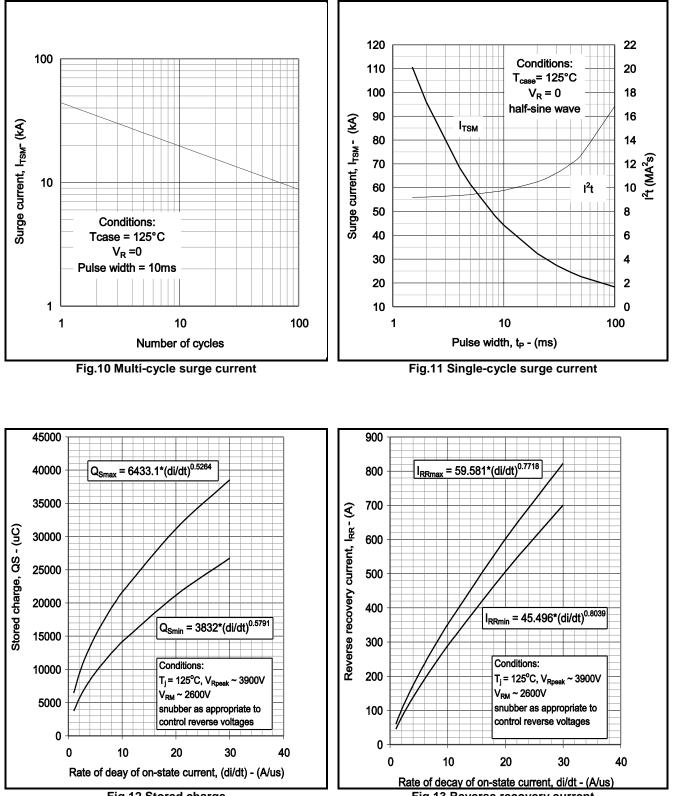


Fig.12 Stored charge

Fig.13 Reverse recovery current



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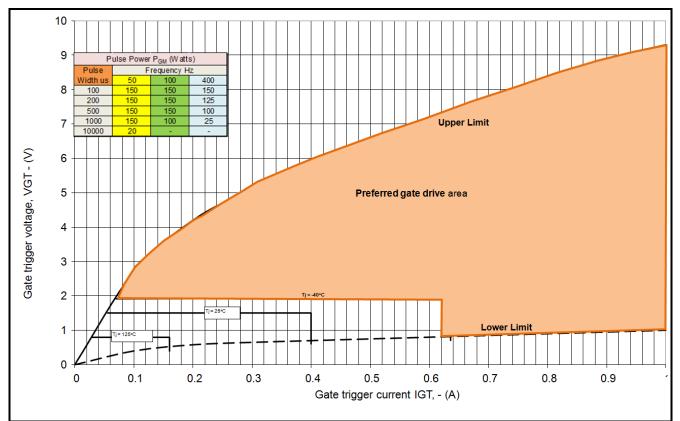


Fig14 Gate Characteristics

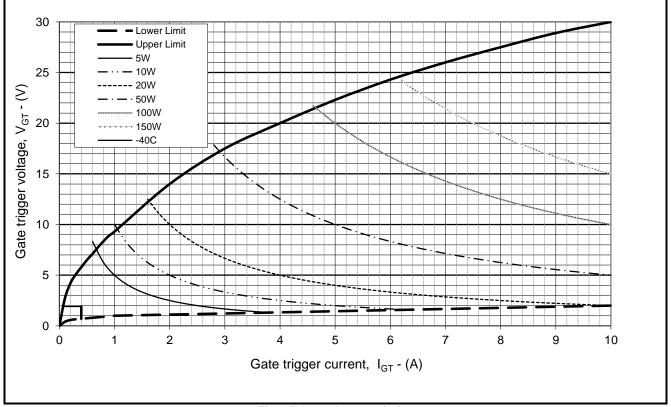


Fig. 15 Gate characteristics



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PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

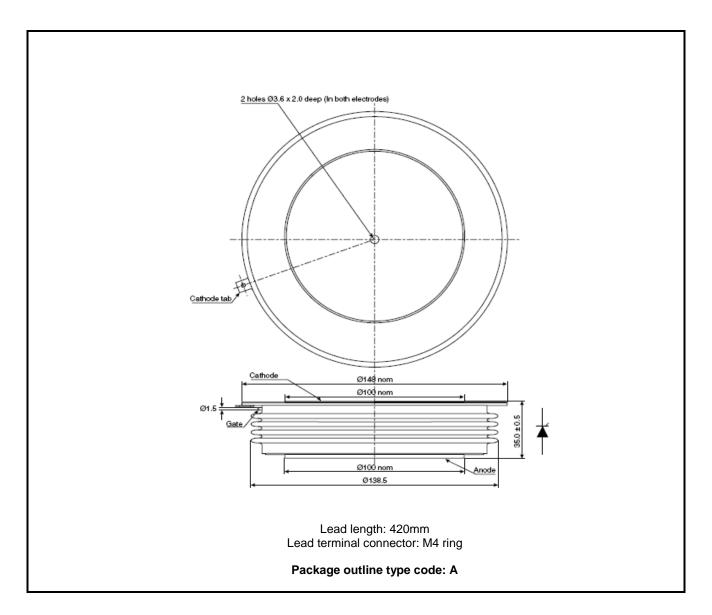


Fig.16 Package outline



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